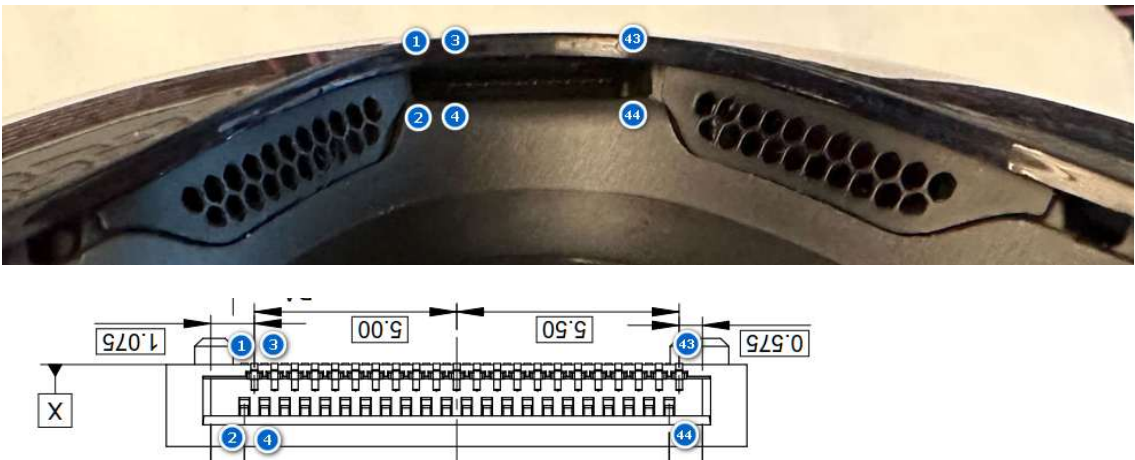


Auxiliary Port – Nose Bridge

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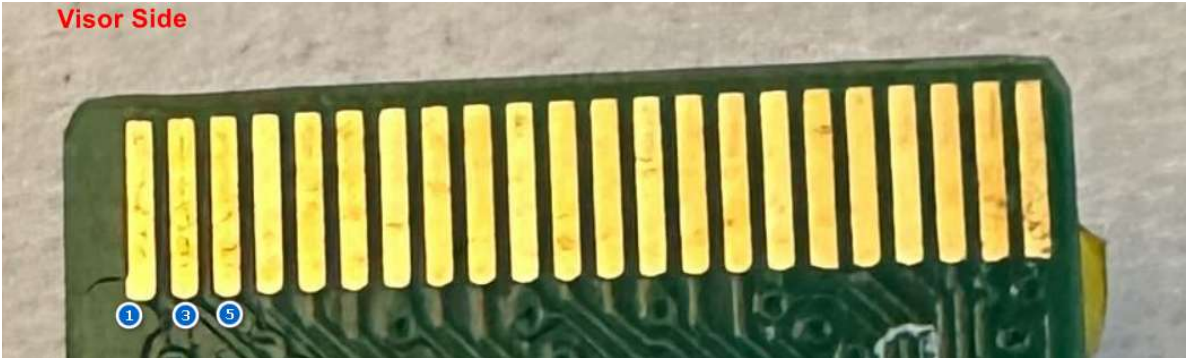
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Pin Order



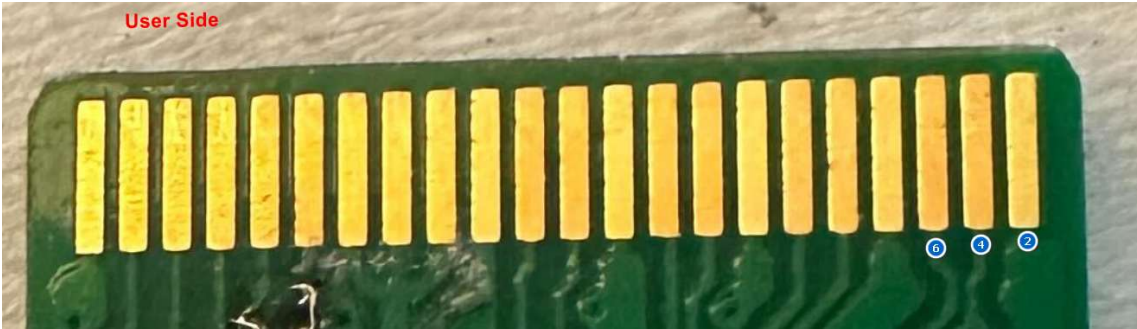
Paddle Interface Top Pads

The mating pads that face the visor side of the connector are shown below. These pads are away from the users' face in normal use.



Paddle Interface Bottom Pads

The mating pads of the user side (board flipped) pin are shown below. These are the pads that are towards the users' face when the headset is being worn.



Pinout

Pin	Name	Type (From the Core)	Description
1	GND	Power Ground	System ground
2	GND	Power Ground	System ground
3	R_L0_P	Analog IO	Right Camera DPHY Data Lane 0 Positive
4	R_CLK_P	Analog IO	Right Camera DPHY Clock Lane Positive
5	R_L0_M	Analog IO	Right Camera DPHY Data Lane 0 Negative
6	R_CLK_M	Analog IO	Right Camera DPHY Clock Lane Negative
7	GND	Power Ground	System ground
8	GND	Power Ground	System ground
9	R_L2_P	Analog IO	Right Camera DPHY Data Lane 2 Positive
10	R_L1_P	Analog IO	Right Camera DPHY Data Lane 1 Positive
11	R_L2_M	Analog IO	Right Camera DPHY Data Lane 2 Negative
12	R_L1_M	Analog IO	Right Camera DPHY Data Lane 1 Negative
13	GND	Power Ground	System ground
14	GND	Power Ground	System ground
15	L_CLK_PCIE_RX_P	Multiplexed Analog IO	Left Camera DPHY Clock Lane Positive PCIE SOC RX Pair Positive (muxed). Input to SOC.
16	R_L3_P	Analog IO	Right Camera DPHY Data Lane 3 Positive
17	L_CLK_PCIE_RX_M	Multiplexed Analog IO	Left Camera DPHY Clock Lane Negative PCIE SOC RX Pair Negative (muxed). Input to SOC.
18	R_L3_M	Analog IO	Right Camera DPHY Data Lane 3 Negative
19	GND	Power Ground	System ground
20	GND	Power Ground	System ground
21	L_L0_PCIE_TX_P	Multiplexed Analog IO	Left Camera DPHY Data Lane 0 Positive PCIE SOC TX Pair Positive (muxed). Output from the SOC – AC coupled in the core.
22	R_MCLK	Digital Output	Right Camera master clock – 19.2MHz / 1.8Vpp
23	L_L0_PCIE_TX_M	Multiplexed Analog IO	Left Camera DPHY Data Lane 0 Negative PCIE SOC TX Pair Negative (muxed). Output from the SOC – AC coupled in the core.
24	L_MCLK_PCIE_CLKREQn	Multiplexed Digital Output	Left Camera master clock – 19.2MHz / 1.8Vpp PCIE CLKREQn signal (muxed). Pulled up to 1.8V through 10K in the core
25	GND	Power Ground	System Ground
26	CAM_TRIGGER_PCIE_WAKEn	Multiplexed Muxed Digital IO	Trigger to the cameras. 470Ohm inline with the signal. PCIE WAKEn signal (when muxed). 470Ohm inline with the signal. Wake is pulled up to 1.8V through 10K.
27	L_L1_PCIE_REFCLK_P	Multiplexed Analog IO	Left Camera DPHY Data Lane 1 Positive PCIE REFCLK pair positive (muxed)
28	3V1_CAM	Power Output	3p1V / 2A current limited supply to the peripheral Not enabled until pin 44 is grounded.
29	L_L1_PCIE_REFCLK_M	Multiplexed Analog IO	Left Camera DPHY Data Lane 1 Negative PCIE REFCLK pair negative (muxed)
30	3V1_CAM	Power Output	3p1V / 2A current limited supply to the peripheral Not enabled until pin 44 is grounded.
31	GND	Power Ground	System Ground
32	3V1_CAM	Power Output	3p1V / 2A current limited supply to the peripheral Not enabled until pin 44 is grounded.
33	L_L2_P	Analog IO	Left Camera DPHY Data Lane 2 Positive
34	CCI_SCL	Digital IO	I2C Clock to the SOC 400kHz – must be pulled to 1.8V on the peripheral with 2.2kΩ
35	L_L2_M	Analog IO	Left Camera DPHY Data Lane 2 Negative
36	CCI_SDA	Digital IO	I2C Data to the SOC 400kHz – must be pulled to 1.8V on the peripheral with 2.2kΩ
37	GND	Power Ground	System Ground
38	R_STROBE	Digital Input	Strobe input from the right cameras to the SOC. 1.8V signal to SOC
39	L_L3_P	Analog IO	Left Camera DPHY Data Lane 3 Positive
40	L_STROBE_PCIE_RESETh	Multiplexed Muxed Digital IO	Strobe input from the left camera. 1.8V signal to SOC PCIE RESETh signal (when muxed). 1.8V signal from SOC
41	L_L3_M	Analog IO	Left Camera DPHY Data Lane 3 Negative
42	CAM_RESET	Digital Output	Reset from the SOC. Low = Reset. High = 1.8V
43	GND	Power Ground	System Ground
44	RGB_DET/GND	Digital Input	Detect pin for the core. Internally pulled-up to 1.8V. Should be tied to GND on the peripheral to enable power.

Signal Multiplexing:

Only the “Left” camera signals are switched out for PCIe – this enables a singular camera to be functional. The high speed multiplexers are HI-Z until a valid detect and probe is performed. These analog muxes have a 27.5GHz 3dB rating and a differential insertion loss of 0.7dB at 2.5GHz. The high speed differential pairs as well as the MCLK/CLKREQ run through muxes with the OE.

The low speed digital signals are not tri-state and will switch between the camera path and the PCIe path. These analog muxes have a 3dB point of 200MHz and an on-state resistance of ~30Ω.

Supported Configurations

- 2 CPHY cameras (with no PCIe) -- but likely needs to be clocked down and never tested / unsupported
- 2 DPHY cameras (with no PCIe) -- supported
- 1 DPHY camera with 1L PCIe gen4 -- supported
- 1 CPHY camera with 1L PCIe gen4 -- unsupported but potentially possible
- 0 Cameras with 1L PCIe gen4 – supported
- 2 DPHY cameras (1x 1L combo mode, 1x 4L DPHY) with 1L PCIe Gen4 – potentially supported, needs development

Mux State	DPHY Channels Availability	PCIe Signals Availability	Low Speed Signal Availability
Mux through DPHY	2x 4L DPHY (2.5Gbps) CSi5 DPHY - Right Clock pair + 4L CSi3 DPHY - Left Clock pair + 4L	None	I2C (CCI) 2x 19.2MHz MCLK 2x Camera Strobe 1x Camera Reset 1x Camera Trigger 1x Camera ULPM
Mux to PCIe	1x 4L DPHY (2.5Gbps) 1x 1L DPHY (2.5Gbps) in combo mode CSi5 DPHY - Right Clock pair + 4L CSi3 DPHY - Left Clock pair + 1L (combo Mode)	1x G4 PCIe PCIe1 – 1 Lane (ref clock + TX + RX) Clock request (Takes Left MCLK) PCIe reset (Takes Left Strobe) PCIe Wake (Takes camera trigger)	I2C (CCI) 1x 19.2MHz MCLK 1x Camera strobe 1x Camera ULPM

Dependencies

Power is not applied to the connector until the detect pin (pin 44) is connected to ground via the peripheral.
Additional power gating is implemented based on validating a known device/configuration:

- Valid I2C for known camera configurations (Arcturus RGB)
- Reset/Strobe R shorted together on the peripheral (pin 38/42) – this is power only or PCIE only
- A valid response on the I2C on either a temp sensor (1001 000) or EEPROM (1010 001) - custom configurations

Without one of the three above probings succeeding, power will be removed from the port.

Camera Probing

The Arcturus RGB camera probing is expecting valid camera configurations (0x34 / 0x20).

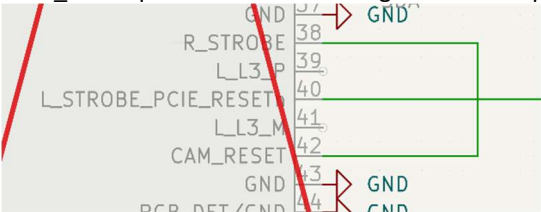
Table 3 I²C Slave Address

SLASEL	I ² C Slave Address
L or NC	0x34(write), 0x35(read)
H	0x20(write), 0x21(read)

These addresses shall be avoided unless using the same image sensors/configurations, or including an EEPROM for additional configuration information.

PCIE or Power Only:

For devices that are PCIE only and need no additional software support, or devices that want power only, the R Strobe and CAM_RESET pins can be shorted together on the peripheral. This enables power to sustain with no additional software/driver work.



All Other Devices:

Any device that needs additional configuration information or driver work (e.g. different camera configurations, a configurable PCIE device, etc.), an EEPROM shall be placed on the I2C bus. A device similar to [CAT24C32](#) is expected.

The supported address is **1010 001**. The base 1010 000 address is consumed by the camera assembly, so that should be avoided.
16b addressing is assumed.

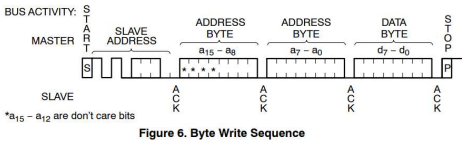


Figure 6. Byte Write Sequence

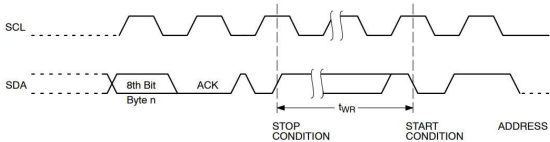


Figure 7. Write Cycle Timing

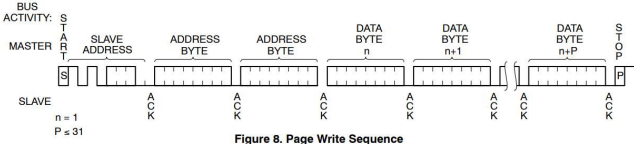


Figure 8. Page Write Sequence

For devices other than the natively supported camera module that use PCIe, the P3T1084 temperature sensor is recommended to be placed on the I2C bus with the address pin tied to GND to give temperature information.

<https://www.nxp.com/docs/en/data-sheet/P3T1084UK.pdf>

Table 4. P3T1084UK address table

No.	Address pin coding	Target address
	A0	
1	GND	1001 000
2	V _{CC}	1001 001
3	SDA	1001 010
4	SCL	1001 011

Additional Details

All digital IO are 1.8V (not differential pairs).

Pull-up resistors of 2.2KΩ to 1.8V for the I2C are required to be added on the peripheral. They are not included on the core as the power-up sequencing of the peripheral can vary and we want to avoid back-driving.

Power

The 3.1V supply is rated to deliver up to 2A continuous. There is a current limit at ~3A.

The early devices had a 1A continuous rated part – this was made a running change to the 2A part at ramp to enable higher current draw.

Do note that the allowable 6W of use will consume over 25% of the available battery capacity, so minimizing consumption is recommended.

There is an internal 700us soft-start.

Output ripple is ~20mVpp with transient response of ±50mV with a 1A step load.

MIPI DPHY Interface

The connector has two different 4L DPHY interfaces are MIPI D-PHY v1.2 with a maximum of 2.5 Gbps/lane

Routing should be implemented at 85Ω differential.

Intrapair length matching should be within 150um

Interpair length matching should be within 350um

Routing length should be minimized to enable maximum data rate.

PCIE Interface

The connector has a single PCIE Gen4 lane exposed. This includes the TX, RX, and CLK differential pairs. All naming is with respect to the core; do not connect the TX from the core to the TX from the peripheral.

PCIE Gen4 is backwards compatible to Gen1, though it will operate at the slowest speed.
<https://pcisig.com/will-pcie-40-products-be-compatible-existing-pcie-1x-pcie-2x-and-pcie-3x-products>

The PCIE Reset, Wake and CLK REQ are 1.8V signals with respect to the core and are **not** 3.3V tolerant. There are 10K pull-ups to 1.8V for WAKE_N and CLKREQ_N on the core. If these need to be translated, that must happen on the peripheral. One example part that has been verified to translate WAKE and CLKREQ with the chipset is [FXWA9306L8X](#).

If RESET needs to be translated, this should also be managed on the peripheral.
Many PCIE devices will internally pull this pin high – please confirm the voltage level.

High-speed Routing should be implemented at 85-90Ω differential.
Intrapair length matching should be within 150um to ensure sufficient signal integrity due to the multiple transitions along the path.

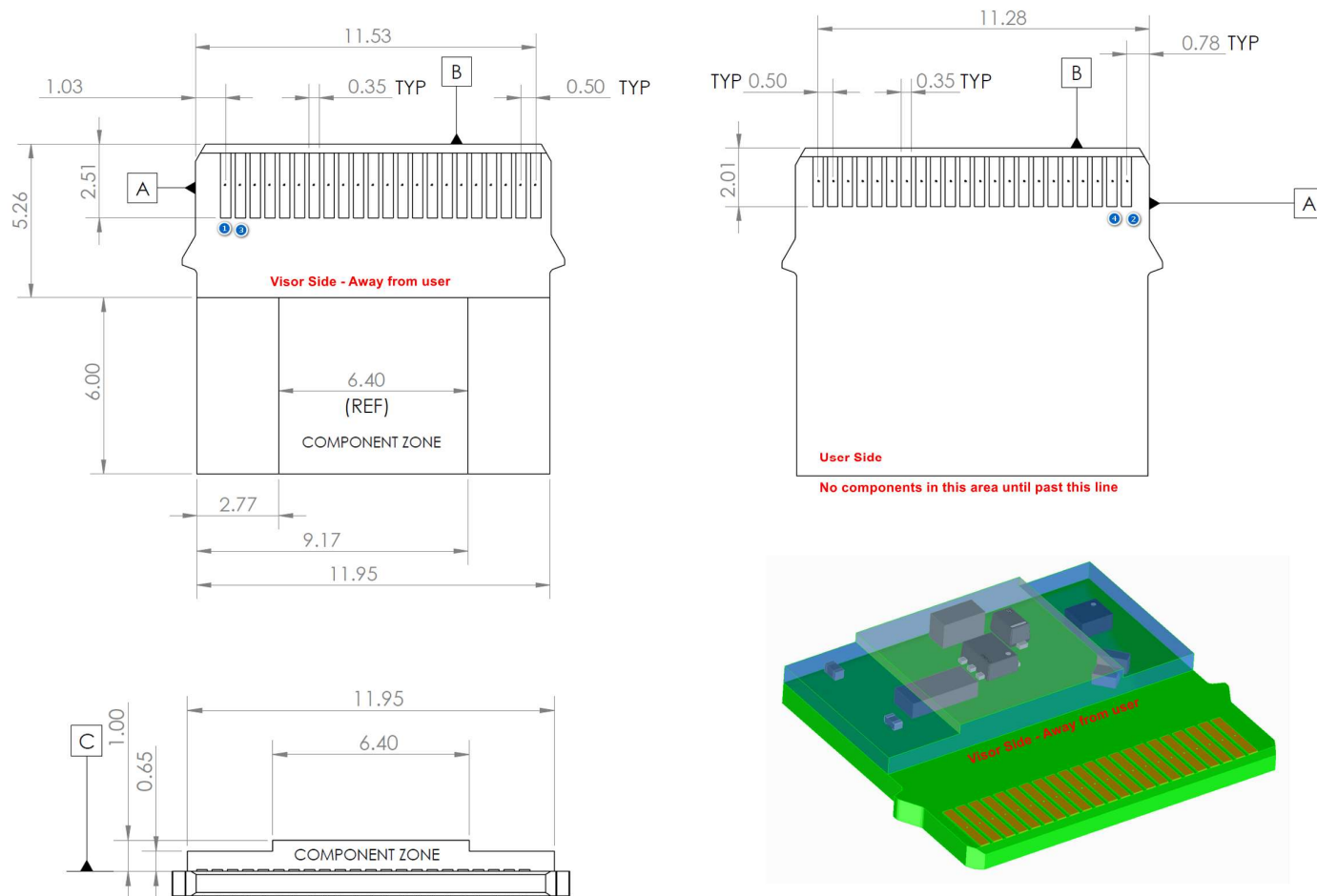
NET	FPC	MB	Seg. L2		Total Length LT	Target Length	[P-M] (mil)	In pair difference	[(TL) - (Rx or Tx)] (mil)	Pair-to-Pair Difference	Impedance
	(A)	(B)	(C)		(E) = (A+B+C+D)			<20mil	(Max. TL) - (D)	<40mil	
SOC_RGB_R_CLK_P	1767.1	3390.31			5157.41	5158.25	4.55	Pass	0.84	Pass	90ohm differential pair R
SOC_RGB_R_CLK_M	1774.14	3378.72			5152.86				5.39	Pass	
SOC_RGB_R_L0_P	1740.27	3388.83			5129.1		0.88	Pass	29.15	Pass	
SOC_RGB_R_L0_M	1754.69	3375.29			5129.98				28.27	Pass	
SOC_RGB_R_L1_P	1736.98	3397.56			5134.54		14.63	Pass	23.71	Pass	
SOC_RGB_R_L1_M	1763.42	3385.75			5149.17				9.08	Pass	
SOC_RGB_R_L2_P	1747.02	3385.03			5132.05		6.07	Pass	26.2	Pass	
SOC_RGB_R_L2_M	1767.46	3370.66			5138.12				20.13	Pass	
SOC_RGB_R_L3_P	1768.41	3389.84			5158.25	5809.38	13.21	Pass	0	Pass	90ohm differential pair L
SOC_RGB_R_L3_M	1768.93	3376.11			5145.04				13.21	Pass	
SOC_RGB_L_CLK_P	1843.94	3711.84	240		5795.78		13.6	Pass	13.6	Pass	
SOC_RGB_L_CLK_M	1856.2	3713.18	240		5809.38				0	Pass	
SOC_RGB_L_L0_P	1827.39	3722.14	240		5789.53		12.16	Pass	19.85	Pass	
SOC_RGB_L_L0_M	1854.66	3707.03	240		5801.69				7.69	Pass	
SOC_RGB_L_L1_P	1804.47	3743.6	240		5788.07		1.31	Pass	21.31	Pass	
SOC_RGB_L_L1_M	1824.17	3725.21	240		5789.38				20	Pass	
SOC_RGB_L_L2_P	2066.08	3742.55			5808.63	5809.38	8.45	Pass	0.75	Pass	
SOC_RGB_L_L2_M	2066.53	3733.65			5800.18				9.2	Pass	
SOC_RGB_L_L3_P	2059.48	3712.03			5771.51		13.32	Pass	37.87	Pass	
SOC_RGB_L_L3_M	2083.67	3701.16			5784.83				24.55	Pass	

Series capacitors are included only on the TX pair (from the core).
The peripheral shall add the necessary capacitors (0.22uF) to its TX lanes (Core RX pair) to meet PCIE compliance.
If the peripheral requires the REFCLK pair to have a DC block, the peripheral shall add those as needed.

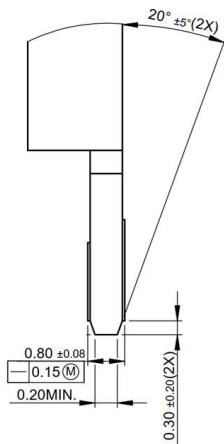
Dimensional Requirements

Pads are 0.5mm pitch, 0.35mm wide.

Pads on the visor side are 2.51mm long, from the board edge, while pads on the user side are 2.01mm long from the board edge. Board edge corners that insert into the connector should be cut at a 45° to help with lead-in.



The board should be 0.8mm thick from pad to pad.
The edge should be chamfered at 20degrees for 0.3mm in depth.



Informative - Reference images of the product assembly:

